MX368033A
CDMA2000 1xEV-DO
Signal Generation Software
Operation Manual
(For MU368030A)

Second Edition

Read this manual before using the equipment.
To ensure that the equipment is used safely, read the "For Safety" in the MG3681A Digital Modulation Generator Operation Manual first.
Keep this manual with the equipment.

ANRITSU CORPORATION

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MX368033A
CDMA 2000 1xEV-DO Signal Generation Software
Operation Manual (For MU368030A)

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Software: MX368033A CDMA2000 1xEV-DO Signal Generation Software

2. Applied Directive and Standards

When the MU368030A universal modulation unit is installed in the MG3681A, the applied directive and standards of this unit is conformed to those of the MG3681A main frame.

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C-tick marking

1. Product Model

Software: MX368033A CDMA2000 1xEV-DO Signal Generation Software

2. Applied Directive and Standards

When the MU368030A universal modulation unit is installed in the MG3681A, the applied directive and standards of this unit is conformed to those of the MG3681A main frame.

PS: About main frame
The kind of main frame (a measuring apparatus) will be to increase. Please, contact us about the newest information of the main frame.

About This Manual

This Operation Manual explains the outline, measurement examples, remote control and other aspects of MX368033A CDMA 2000 1xEV-DO Signal Generation Software. This software is designed to be installed in the MU368030A Universal Modulation Unit mounted on the MG3681A Digital Modulation Signal Generator.

[ ] represents a panel key.
The MG3681A Digital Modulation Signal Generator Operation Manual and the MU368030A Universal Modulation Unit Operation Manual are available as separate volumes.
Use them in conjunction with this Operation Manual.

Table of Contents

IV.

Section 1 Overview

This section describes the outline and product configuration of MX368033A CDMA2000 1xEV-DO Signal Generation Software product and standard accessories.

1.1 Product Overview

The MX368033A CDMA2000 1xEV-DO Signal Generation Software (hereinafter, referred to as this software) is system software to be installed in the MU368030A Universal Modulation Unit.
To use this software, a Universal Modulation Unit must be mounted on the MG3681A Digital Modulation Signal Generator.

By installing this software, you can output modulation signals according to CDMA2000 1xEV-DO specifications, not using an external baseband signal source.

1.2 Product Configuration

Standard configuration of the MX368033A is given in the table below. After unpacking, check that all items listed are included. If any items are missing or damaged, please contact Anritsu or one of our agencies.

Items	Model name/type	Product name	Quan-tity	Remarks
Main unit	MX368033A	CDMA2000 1xEV-DO Signal Generation Software	1	Supplied with Compact Flash or ATA Flash card.
Accessories		PC card adapter	1	Supplied only with Compact Flash card.
		CDMA2000 1xEV-DO Signal Generation Software Signal Pattern Files	1	Supplied with CD-R.
	M-W2072AE	Operation Manual	1	

Section 2 Operation Outline

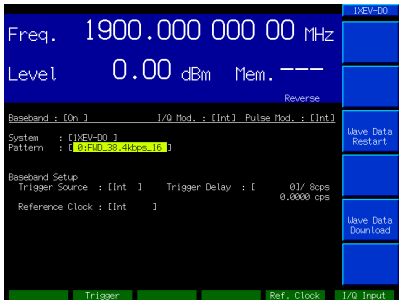
This section describes basic screen contents and how to input auxiliary signals when mounting the MU368030A Universal Modulation Unit installed with this software onto the MG3681A.

2.1 Screen Transitions

The screens are transited as shown below:

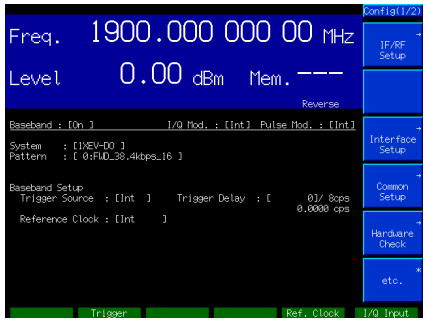
Press main function key [●Digital Mod] .

Digital modulation setup screen

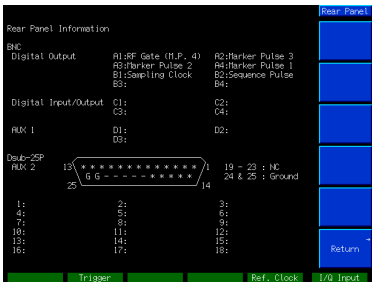


Press main function key [● Config] .

Environment setup screen

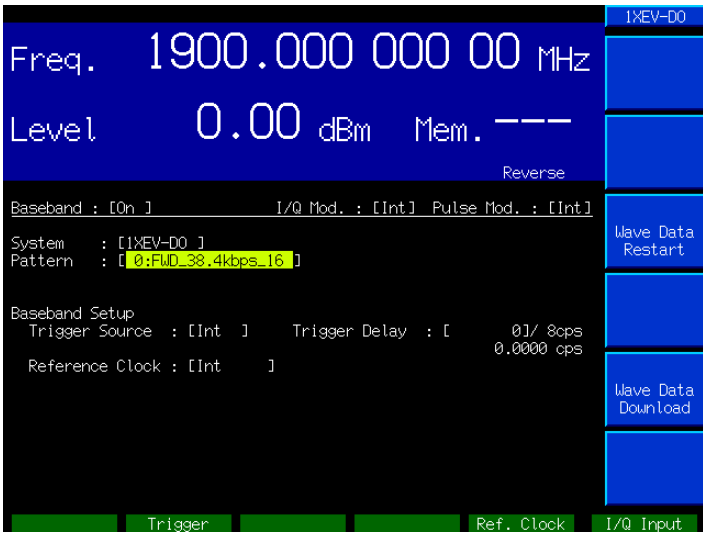


Rear Panel Information screen



2.2 Setting Modulation Parameters

Pressing [Digital Mod] causes the indicator LED to go on and the Main screen to appear. Basic parameters related to digital modulation can be set on this screen. This section describes settings for the Main screen.



[1] Baseband

Select On/Off for the operation of the Baseband Signal Generator Unit.

[2] I/Q Mod.

Select the I/Q signal source for orthogonal modulation. Select "Int" to use the internal signal source for the I/Q signal (using this software) or "Ext" to use the external input.

Initial value: Int

[3] Pulse Mod.

Set the modulation signal on the pulse modulator.

Int: Selects the control signal generated by this software.

Ext: Uses the external input signal for pulse modulation regardless of modulation settings.

Off: No pulse modulation

[4] System

Set the system software. Select "1xEV-DO" to start this software.

[5] Pattern

Select the 1xEV-DO modulation signal. For selectable 1xEV-DO modulation signal, refer to "1xEV-DO modulation signal list" in Section 3.1.1.

[6] Trigger Source

Switches the inside and the outside of modulation signal transmitting timing. For details, refer to Section 3.3.

Int: Outputs a RF signal in synchronization with a internal trigger signal.

Start: Transmits a modulation signal using an external signal as the start signal.

Frame: Transmits a modulation signal using an external signal as a frame trigger. (Not used in this software.)

Initial value: Int

[7] Trigger Delay

Sets the output signal delay for the trigger signal input to the Start TRIG connector.

For details, refer to Section 3.3.

Setting range: 0 to 16777215

Initial value: 0

[8] Reference Clock

Int: Generates the reference clock inside MG3681A.

Ext (TTL): Inputs the reference clock from the outside. (The Ref. Clock connector is used.) In this case, set this connector to TTL mode.

Ext (AC) : Same as Ext (TTL) except that the Ref. Clock connector mode should be set to AC (5 Vp-p).

[9] Wave Data Restart

Pressing this button while Trigger Source is set to Start allows synchronization with the external trigger again.

[10] Wave Data Download

The 1xEV-DO modulation wave data can be re-installed. For details, refer to Section 2.4.

2.3 Inputting Auxiliary Signal

2.3.1 Inputting external trigger signal

You can synchronize the signal input at digital signal input connector No. 2,"Trigger," on the front panel of the MG3681A with the RF output timing. For details, refer to Section 3.3.

2.3.2 Inputting external reference clock signal

You can synchronize the signal input at digital signal input connector No. 5, "Ref. Clock," on the front panel of the MG3681A with the internal reference clock of the baseband signal. A 9830.4 kHz-signal that is 8 times of the chip rate (1228.8 ksps) can be input as the external reference clock. When using the 10/13 MHz Ref Input on the MG3681A main unit, both the RF and baseband signals are synchronized with the external input. However, when using this input, the RF signal remains to be synchronized with internal 10 MHz. The input frequency of external reference clock should be 9830.4 kHz ±5%.

Relationship between the external reference clock settings and output signal reference clock is shown below.

Table 2-1 Relationship between External Reference Clock and Output Signal Reference Clock

External Reference Clock Settings		Output Signal Reference Clock	
Reference Clock	10/13 MHz Ref Input	Baseband Signal	RF Signal
Int	Int	Internal Reference	Internal Reference
Int	Ext	Ext 10/13 MHz Ref Input	Ext 10/13 MHz Ref Input
Ext	Int	Ext Ref.Clock	Internal Reference
Ext	Ext	Ext Ref.Clock	Ext 10/13 MHz Ref Input

2.4 Downloading Signal Pattern Files of MX368033A

It is available to download signal pattern files of 1xEV-DO modulation signal. First, insert the attached memory card, in which signal pattern files to be downloaded are saved, into the PC-card slot on the rear panel of the MG3681A. Then, press F5 (Wave Data Download) in the Digital Modulation Parameter Setting Screen. Selecting “yes” in the Selecting window starts downloading. It takes approximately 12 minutes until completion. Do not cut power off while downloading is in progress.

Section 3 Details of Functions

This section details the MX368033A CDMA2000 1xEV-DO Signal Generator Software functions.

3.1 1xEV-DO Modulation Signal

3.1.1 Overview of 1xEV-DO modulation signal

The 1xEV-DO modulation signal can be selected as a Pattern. The available 1xEV-DO modulation signals are shown below.

FWD_38.4_16_MR/…/FWD_2457.6_1_MR

When those 1xEV-DO signals are selected, the CDMA2000 1xEV-DO forward modulation signal, where channel coding, TDM modulation and IQ mapping are conducted according to 3GPP2 C.S0024, is output.

FWD_Idle_Slot_MR

When this 1xEV-DO signal is selected, the CDMA2000 1xEV-DO forward idle slot modulation signal, where TDM modulation and IQ mapping are conducted according to 3GPP2 C.S0024, is output.

RVS_9.6 kbps/…/RVS_153.6 kbps_RT

When these 1xEV-DO signals are selected, the CDMA2000 1xEV-DO reverse modulation signal, where channel coding and IQ mapping are conducted according to 3GPP2 C.S0024, is output.

A list of the 1xEV-DO modulation signals is shown below.

Table 3-1 1xEV-DO Modulation Signal List

No.	1xEV-DO Modulation Signal	Applicable System	Baseband Filter	Data
0	FWD_38.4_16_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
1	FWD_76.8_8_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
2	FWD_153.6_4_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
3	FWD_307.2_2_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
4	FWD_614.4_1_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
5	FWD_307.2_4_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
6	FWD_614.4_2_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
7	FWD_1228.8_1_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
8	FWD_921.6_2_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
9	FWD_1843.2_1_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
10	FWD_1228.8_2_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
11	FWD_2457.6_1_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	PN15fix*
12	FWD_Idle_Slot_MR	CDMA2000 1xEV-DO Forward	IS-95SPEC +EQ	-
13	RVS_9.6 kbps	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
14	RVS_19.2 kbps	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
15	RVS_38.4 kbps	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
16	RVS_76.8 kbps	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
17	RVS_153.6 kbps	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*

* Data length is not an integer multiple of the PN sequence length (32767 bits for PN15 or 511 bits for PN9). The PN sequences are thus discontinuous at the data end.

Table 3-1 1xEV-DO Modulation Signal List (Continuous)

No.	1xEV-DO Modulation Signal	Applicable System	Baseband Filter	Data
19	RVS_9.6 kbps_RT	CDMA2000 1xEV-DO Forward	IS-95SPEC	PN9fix*
20	RVS_19.2 kbps_RT	CDMA2000 1xEV-DO Forward	IS-95SPEC	PN9fix*
21	RVS_38.4 kbps_RT	CDMA2000 1xEV-DO Forward	IS-95SPEC	PN9fix*
22	RVS_76.8 kbps_RT	CDMA2000 1xEV-DO Forward	IS-95SPEC	PN9fix*
23	RVS_153.6 kbps_RT	CDMA2000 1xEV-DO Forward	IS-95SPEC	PN9fix*

* Data length is not an integer multiple of the PN sequence length (32767 bits for PN15 or 511 bits for PN9). The PN sequences are thus discontinuous at the data end.

3.2 Modulation Signal Details

This section describes the 1xEV-DO forward, 1xEV-DO reverse and 1xEV-DO forward idle slot modulation signal configurations.

3.2.1 1xEV-DO forward (without FWD_Idle_Slot_MR)

When a 1xEV-DO modulation signal from FWD_38.4_16_MR to FWD_2457.6_1_MR for Pattern is selected, the CDMA2000 1xEV-DO forward modulation signal where channel coding and IQ mapping are conducted according to 3GPP2 C.S0024, is output. The pilot, forward MAC and forward traffic channels are multiplexed on this output signal. For the forward traffic channel, PN15fix* is used as the data before adding FCS (Frame check sequence.) The bit string format, after adding FCS and TAIL bit strings to the PN15fix bit string is shown in Figure 3-1. The bit string after adding FCS and TAIL bit strings to the PN15fix bit string is called a packet in this manual.

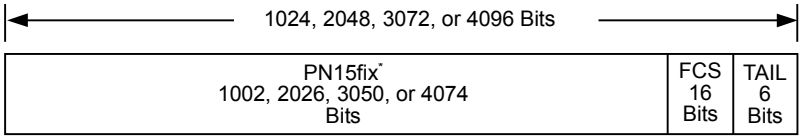


Figure 3-1 Forward Packet Format

A packet goes through TDM (Time Division Multiplex) with other channels after channel coding including turbo-cording, scramble, channel interleaving and modulation (QPSK, 8-PSK, 16QAM), etc. The MACIndex used for scrambling is the same value as MACIndex used by the preamble in the same slot.

* Data length is not the integer multiple of the PN sequence length (32767 bits for PN15). The PN sequences are thus discontinuous at the data end.

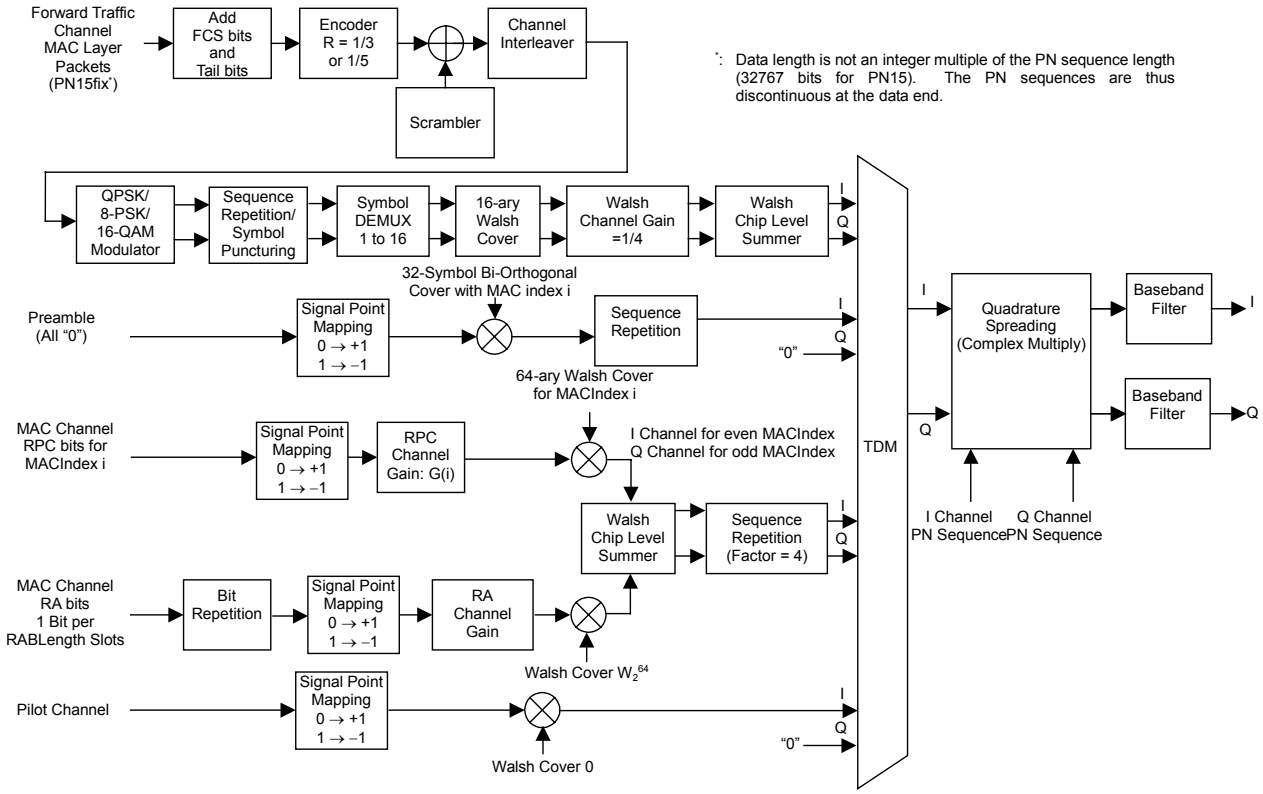


Figure 3-2 1xEV-DO Forward Block Diagram

A packet after channel coding is then allocated to a data area in a slot together with a preamble with the same MACIndex during Time Division Multiplex. The slot format is shown in Figure 3-3. Time Division Multiplex status for preamble, packet after channel-coding, MAC channel and pilot channel are shown in Figure 3-4.

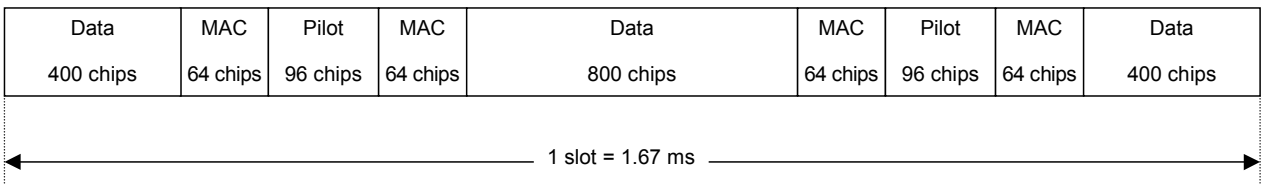


Figure 3-3 Slot Format of 1xEV-DO Forward (without idle slot)

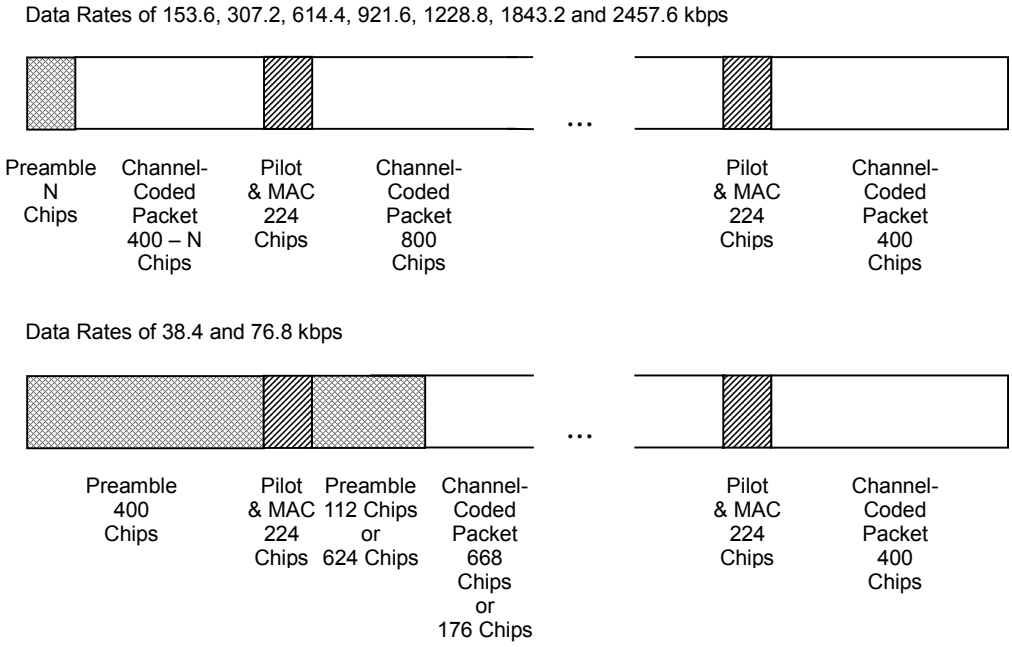


Figure 3-4 Timing Diagram

4 PN15fix data with different initial values on the PN15 code generator as data for the forward traffic channel are created. Then a packet is created from each PN15fix data. Each packet goes through channel coding. The MACIndex values used by the scrambler differ according to each packet. (The same MACIndex as the packet is used for the preamble allocated to the slot together with that packet. For MACIndex values, refer to Figure 3-5.) A channel-coded packet is allocated to a slot in 3-slot intervals. Other packets that have gone through channel coding are allocated to the 3 intermediate slots. An example where forward traffic channels are allocated in 3-slot intervals is shown in Figure 3-5 while the forward traffic channel parameters are shown in Table 3-2.

Table 3-2 Traffic Channel Parameters

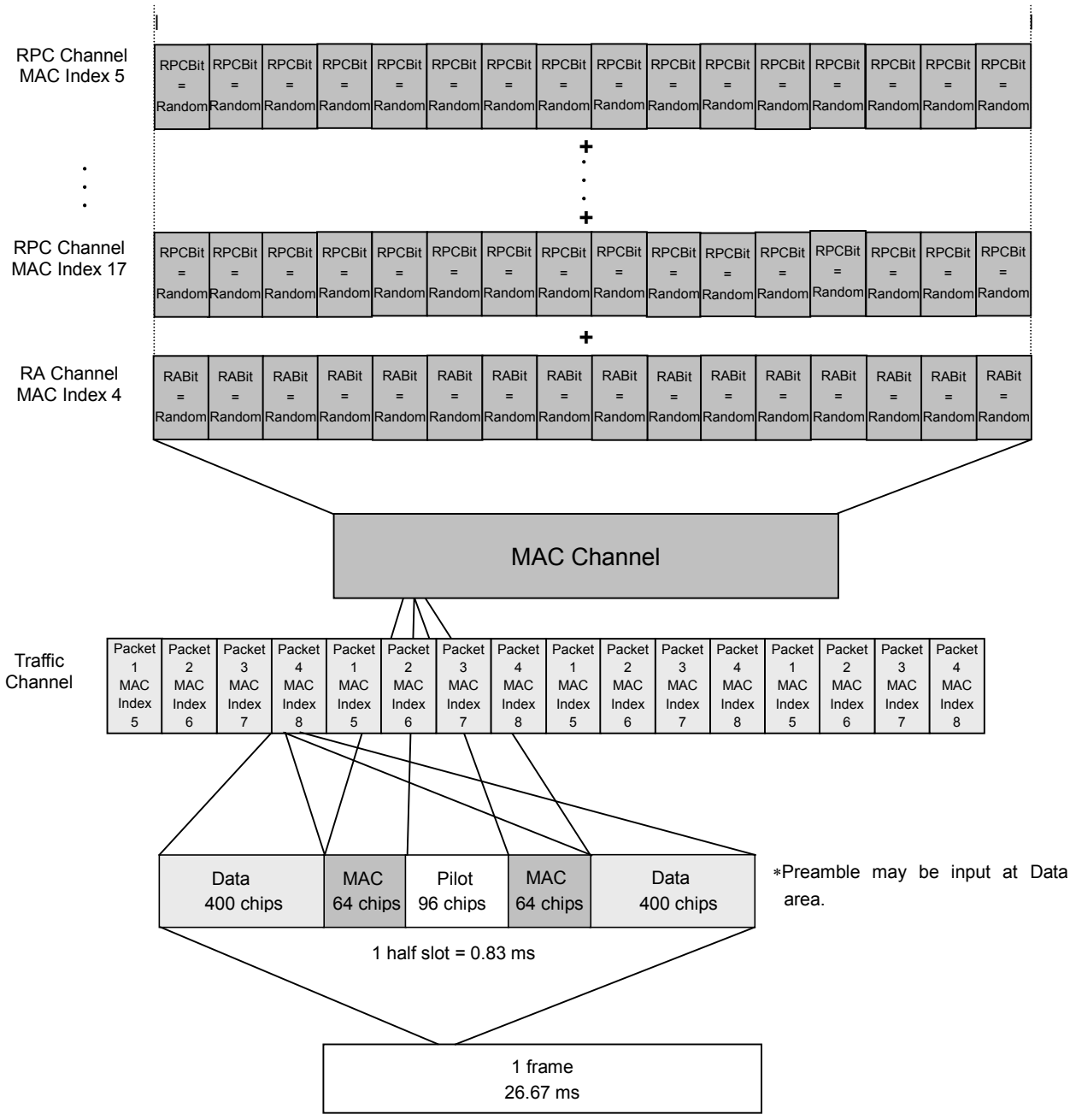
No.	1xEV-DO Modulation Signal	Data Rate (kbps)	Slot	Packet (Bit)	Preamble (Chip)	Modulation Type
0	FWD_38.4_16_MR	38.4	16	1024	1024	QPSK
1	FWD_76.8_8_MR	76.8	8	1024	512	QPSK
2	FWD_153.6_4_MR	153.6	4	1024	256	QPSK
3	FWD_307.2_2_MR	307.2	2	1024	128	QPSK
4	FWD_614.4_1_MR	614.4	1	1024	64	QPSK
5	FWD_307.2_4_MR	307.2	4	2048	128	QPSK
6	FWD_614.4_2_MR	614.4	2	2048	64	QPSK
7	FWD_1228.8_1_MR	1228.8	1	2048	64	QPSK
8	FWD_921.6_2_MR	921.6	2	3072	64	8-PSK
9	FWD_1843.2_1_MR	1843.2	1	3072	64	8-PSK
10	FWD_1228.8_2_MR	1228.8	2	4096	64	16QAM
11	FWD_2457.6_1_MR	2457.6	1	4096	64	16QAM

MAC channel parameters are shown in Table 3-3.

Table 3-3 MAC Channel Parameters

MACIndex	RABit	RPCBit
4(RA Channel), 5-17(RPC Channel)	Random	Random

The RPCBit to be put on the RPC channel is arranged at random, while the RABit to be put on the RAChannel are at random. There are 13 RPC channels and one RA channel. Each MAC channel is spread by the Walsh Cover depending on MACIndex, and then multiplexed. A MAC channel is allocated to the MAC area in a slot as shown in Figure 3-3. The relationship between MAC channel, data sent from the traffic channel and slot is shown in Figure 3-5.



*Preamble may be input at Data area.

Figure 3-5 Multiplexing of each Channel

3.2.2 1xEV-DO reverse

When a 1xEV-DO modulation signal from RVS_9.6 kbps to RVS_153.6 kbps_RT is selected for Pattern, the CDMA2000 1xEV-DO reverse modulation signal where channel coding and IQ mapping are conducted according to 3GPP2 C.S0024, is output. The pilot, RRI, DRC, ACK and data channels are multiplexed on this output signal. For the Data Channel, PN9fix* is used as the data before FCS (Frame check sequence) is added. The bit string format after FCS and TAIL bit strings are added to the PN9fix bit string is shown in Figure 3-6.

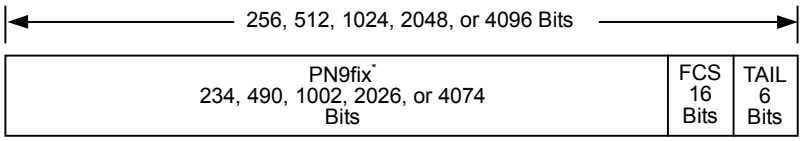


Figure 3-6 Reverse Packet Format

The bit string after adding FCS and TAIL bit strings to the PN9fix bit string is multiplexed with the pilot, RRI, DRC and ACK channels after channel coding. The block diagram of 1xEV-DO is shown in Figure 3-7. Modulation parameters and channel gains for each are shown in Table 3-4 and 3-5, respectively.

* Data length is not an integer multiple of the PN sequence length (511 bits). The PN sequences are thus discontinuous at the data end.

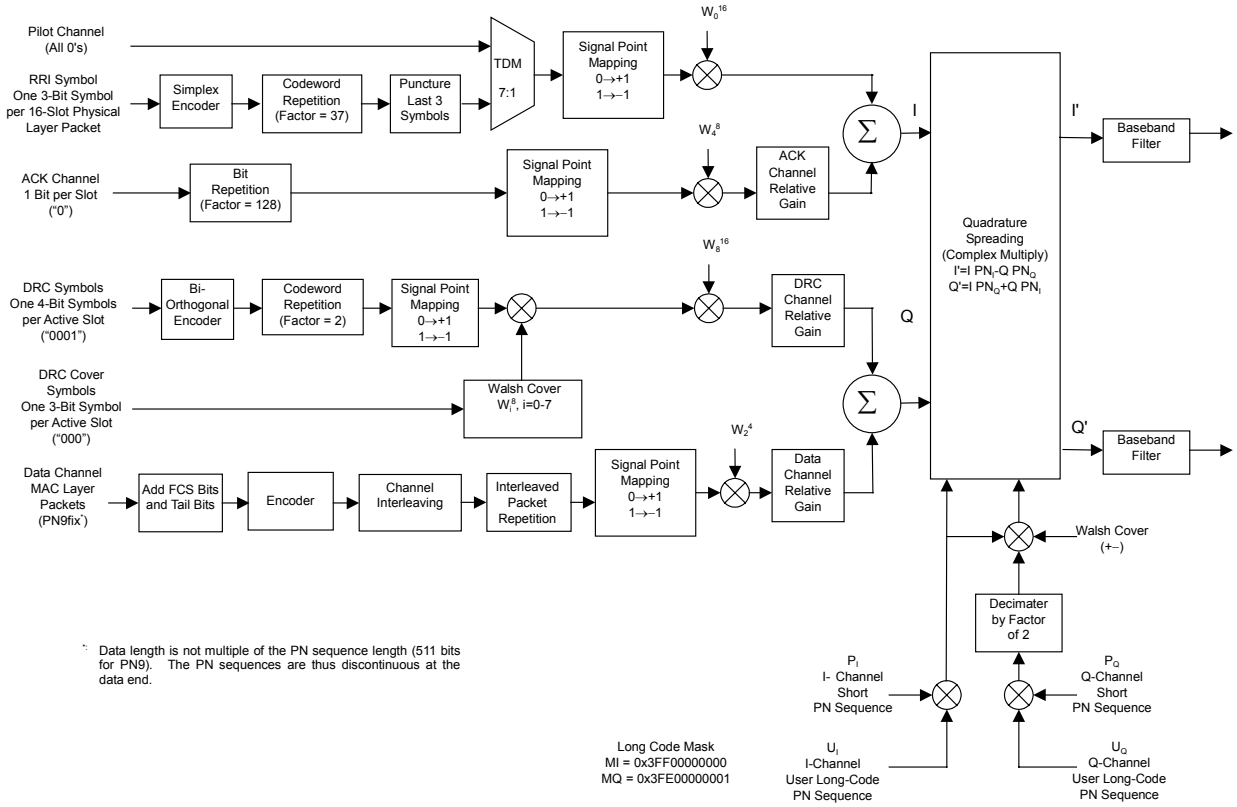


Figure 3-7 1xEV-DO Reverse – Block Diagram

Table 3-4 Reverse Modulation Parameters

No.	1xEV-DO Modulation Signal	Data Rate (kbps)	RRI Symbol	DRC Value	DRC Cover	ACK Channel Bit	Long Code Mask
13	RVS_9.6 kbps	9.6	001	0x01	W_0^8	0	MI = 0x3FF00000000 MQ = 0x3FE00000001
14	RVS_19.2 kbps	19.2	010	0x01	W_0^8	0	
15	RVS_38.4 kbps	38.4	011	0x01	W_0^8	0	
16	RVS_76.8 kbps	76.8	100	0x01	W_0^8	0	
17	RVS_153.6 kbps	153.6	101	0x01	W_0^8	0	
19	RVS_9.6 kbps_RT	9.6	001	0x01	W_0^8	0	
20	RVS_19.2 kbps_RT	19.2	010	0x01	W_0^8	0	
21	RVS_38.4 kbps_RT	38.4	011	0x01	W_0^8	0	
22	RVS_76.8 kbps_RT	76.8	100	0x01	W_0^8	0	
23	RVS_153.6 kbps_RT	153.6	101	0x01	W_0^8	0	

Table 3-5 Reverse Channel Gain

No.	1xEV-DO Modulation Signal	Data Rate (kbps)	Data/ Pilot	RRI/ Pilot	DRC/Pilot	ACK/Pilot
13	RVS_9.6 kbps	9.6	3.75 dB	0 dB	3.0 dB	3.0 dB
14	RVS_19.2 kbps	19.2	6.75 dB	0 dB	3.0 dB	3.0 dB
15	RVS_38.4 kbps	38.4	9.75 dB	0 dB	3.0 dB	3.0 dB
16	RVS_76.8 kbps	76.8	13.25 dB	0 dB	3.0 dB	3.0 dB
17	RVS_153.6 kbps	153.6	18.50 dB	0 dB	3.0 dB	3.0 dB
19	RVS_9.6 kbps_RT	9.6	3.75 dB	0 dB	3.0 dB	0 dB
20	RVS_19.2 kbps_RT	19.2	6.75 dB	0 dB	3.0 dB	0 dB
21	RVS_38.4 kbps_RT	38.4	9.75 dB	0 dB	3.0 dB	0 dB
22	RVS_76.8 kbps_RT	76.8	13.25 dB	0 dB	3.0 dB	0 dB
23	RVS_153.6 kbps_RT	153.6	18.50 dB	0 dB	3.0 dB	0 dB

3.2.3 1xEV-DO forward idle slot

When FWD_Idle_Slot_RT is selected for Pattern, the CDMA2000 1xEV-DO forward idle slot modulation signal where IQ mapping is conducted according to 3GPP2 C.S0024, is output. The pilot and forward, MAC channels are multiplexed on this output signal. RABit is "0" in all slots. The block diagram of the forward idle slot is shown below.

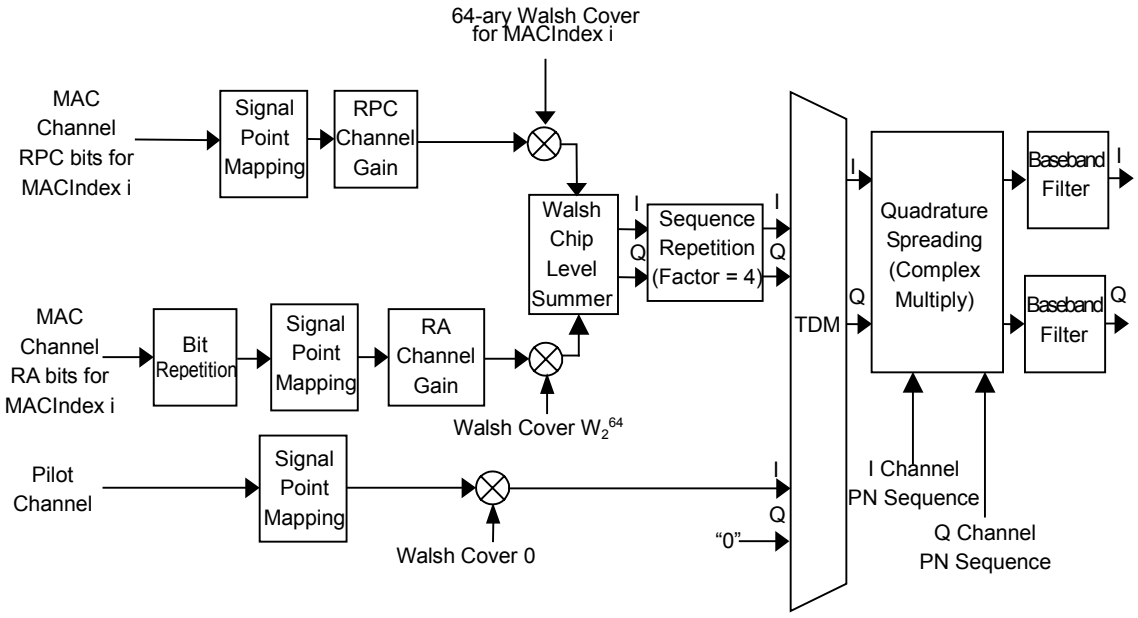


Figure 3-8 Forward Idle Slot – Block Diagram

The forward idle slot format is shown in Figure 3-9. MAC channel parameters for the forward idle slot are shown in Table 3-6.

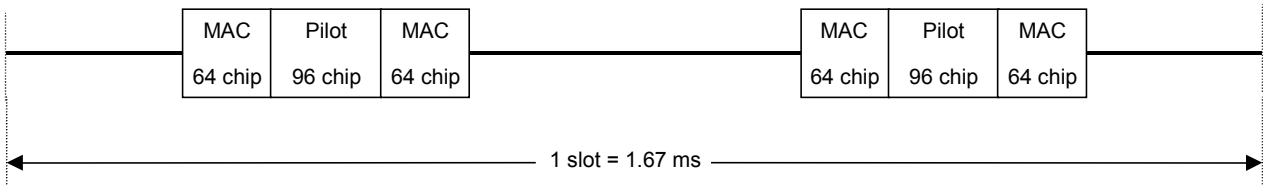


Figure 3-9 1xEV-DO Forward Idle Slot Format

Table 3-6 MAC Channel for Forward Idle Slot

MAC Index	RA Bit	RPC Bit	RA Channel Gain	RPC Channel Gain
4 (RA Channel), 5-17 (RPC Channel)	Random	Random	–12.04 dB*	–11.42 dB*

* Relative values for Pilot Channel

3.3 External Trigger Input

RF signal output timing for trigger signal inputs to the Start TRIG input (front panel) to synchronize with other devices is shown in the figure below. The RF signal is output with a delay of 9/8 chips (1 chip = 1/1228.8 ms) plus trigger delay set value from the trigger rise edge. The actual delay from Start TRIG input is as shown in the expression given below, as the RF output timing includes an error of ±2/16 chips.

(Delay from Start TRIG input) =
9/8 chips + (Trigger Delay) ± (Delay error)

Start TRIG input level is TTL.

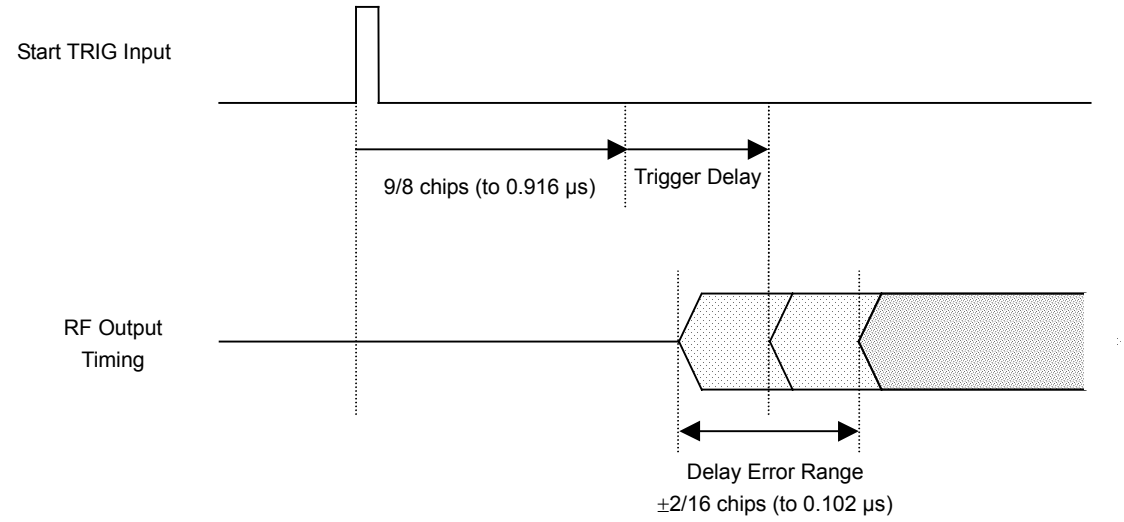


Figure 3-10 External Trigger Operation

3.4 Frame Trigger Output

The Frame Trigger (A4) and Sequence Pulse (B2) are output from the BNC connector on the rear panel of the MG3681A. For the output timing of Frame Trigger, Sequence Pulse and RF output, refer to Figures 3-11 through 3-13.

Frame Trigger

The Frame Trigger is a TTL-level pulse signal synchronized with a 26.67-ms 1xEV-DO frame. The pulse width is 1/8 chip. It is output from the A4 connector on the rear panel of the MG3681A.

Sequence Pulse

Sequence Pulse is a TTL-level pulse signal synchronized with the PN15fix repeat period when 1xEV-DO forward is selected for Pattern. It is synchronized with the PN9fix repeat period when 1xEV-DO reverse is selected, and it is synchronized with the 1xEV-DO frame when 1xEV-DO modulation signal FWD_Idle_Slot_RT is selected. The pulse width is 1/8 chip. It is output from the B2 connector on the rear panel of the MG3681A.

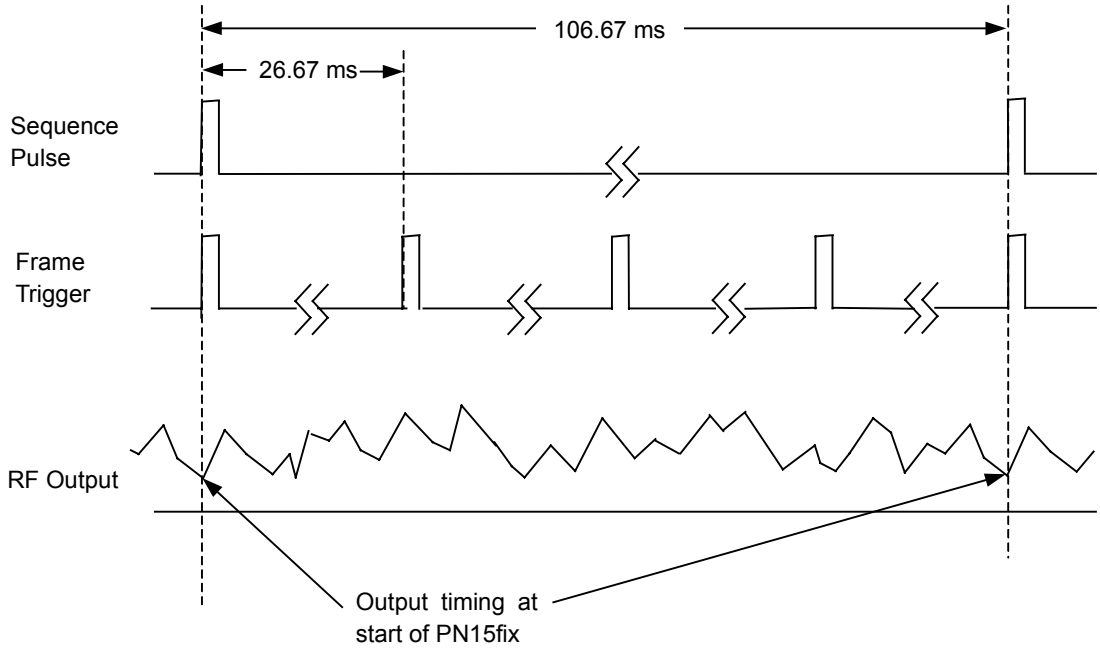


Figure 3-11 Trigger Timing for Forward (excluding Idle Slot)

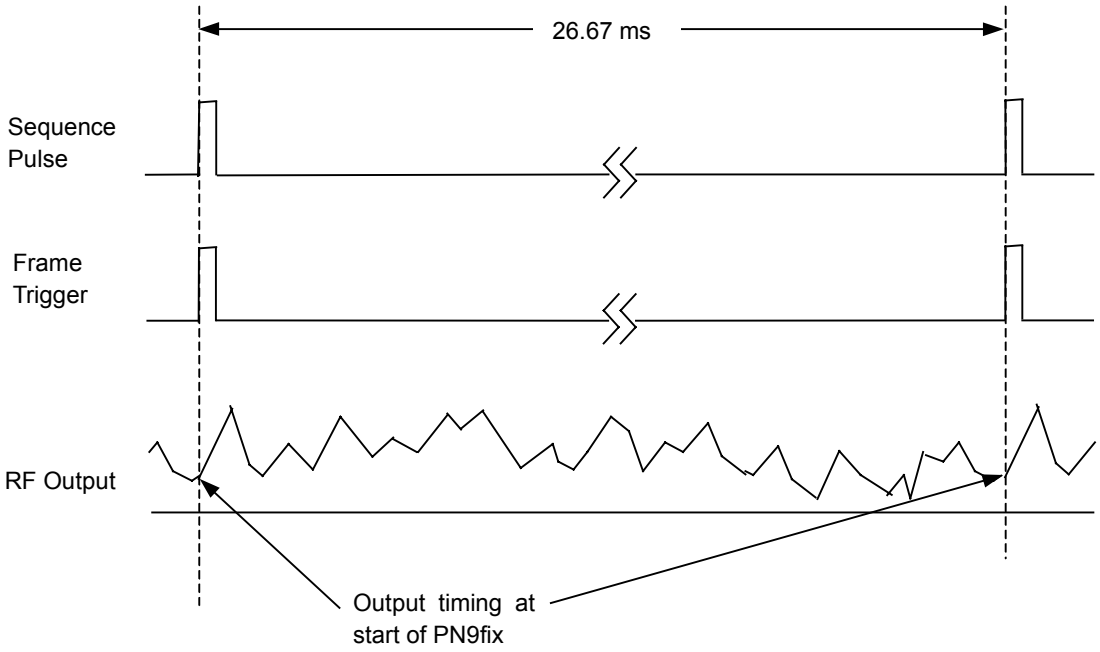


Figure 3-12 Reverse Trigger Timing

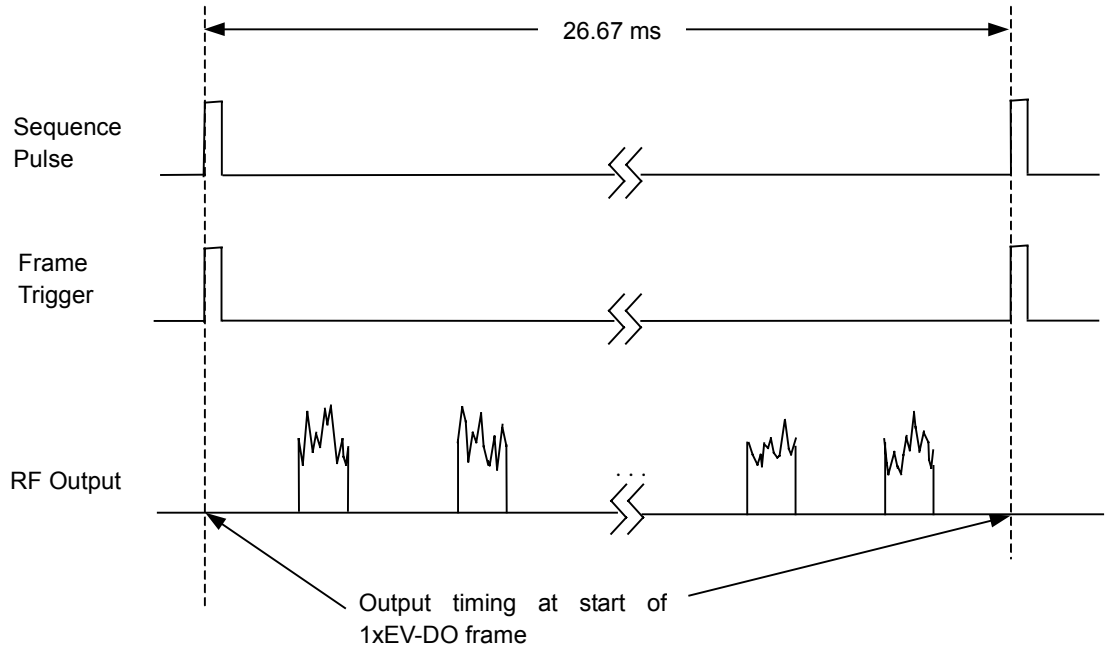


Figure 3-13 Trigger Timing for Forward Idle Slot

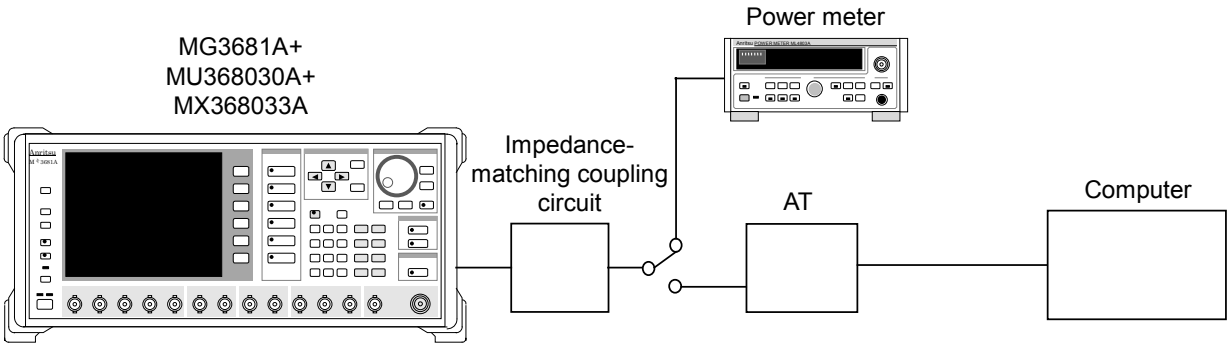
Section 4 Measurement

This section explains each PER measurement of a Access Terminal (AT) receiver and Access Network (AN) receiver, as an example of measurement when mounting the MU368030A Universal Modulation Unit with MX368033A CDMA2000 1xEV-DO signal generation software onto the MG3681A Digital Modulation Signal Generator.

4.1 PER Measurement of AT Receiver

This section explains PER (Packet Error Rate) measurement of AT receiver. It explains as aim for receiver which enables setting of the receiving mode of traffic channel and reading of PER data with a computer, etc., without using the call processing.

Setup



Measuring procedures

[1] Set the frequency and output level of the MG3681A to desired value.

[2] Set the modulation system of the MG3681A to "1xEV-DO."

[3] Set the measured 1xEV-DO modulation signal to Pattern of the MG3681A.

[4] Connect RF output of the MG3681A to the power meter trough the impedance-matching coupling circuit. Then, adjust the output level of the MG3681A to obtain the sensitivity test level with the power meter.

[5] Switch output of impedance-matching coupling circuit to the AT.

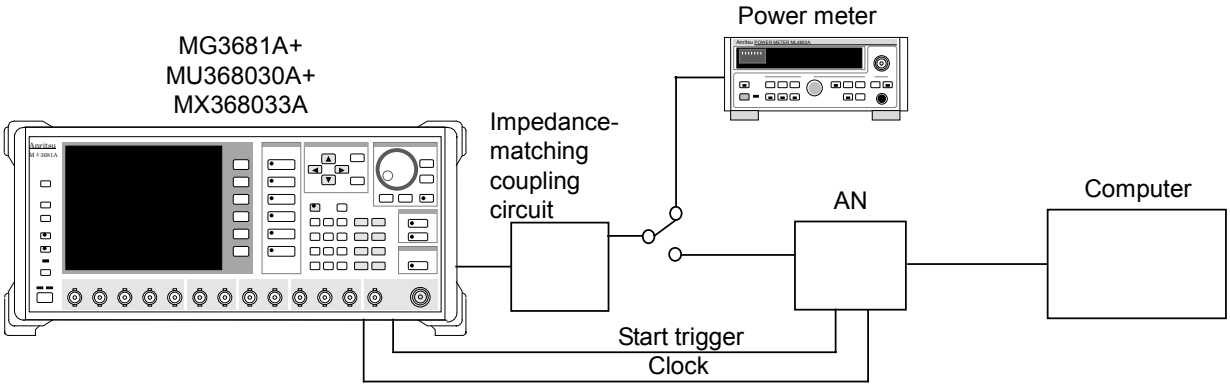
[6] Set AT to the receiving mode using the computer.

[7] Obtain the PER data from the AT using the computer.

4.2 PER Measurement of AN Receiver

This section explains PER (Packet Error Rate) measurement of AN receiver. It explains as the object: the receiver which enables setting of the receiving mode of data channel and reading of PER data with a computer, etc., without using the call processing. In this case, it is needed that the start trigger synchronized with reference clock of 10 MHz or 9.8304 MHz, and 1xEV-DO frame, is output from AN.

Setup



Measuring procedures

[1] Set the frequency and output level of the MG3681A to desired value.

[2] Set the modulation system of the MG3681A to "1xEV-DO."

[3] Set the measured 1xEV-DO modulation signal to Pattern of the MG3681A.

[4] Connect the RF output of the MG3681A to the power meter through the impedance-matching coupling circuit. Then, adjust the output level of the MG3681A to obtain the sensitivity test level with the power meter.

[5] Switch output of impedance-matching coupling circuit to the AN.

[6] Synchronize the built-in Reference Clock of the MG3681A with the AN.
Set Trigger Source to "Start." As for Reference Clock, set "Ext" for use of Ref Clock and "Int" for use of 10/13MHz Ref Input respectively.

[7] Set the receiver to the receiving mode using the computer.

[8] Set Trigger Delay of the MG3681A to appropriate value.

[9] Re-synchronize the MG3681A with the AN by pressing Wave Data Restart of the MG3681A.

[10] Obtain PER data from the AN receiver using the computer.

Section 5 Remote Control

This section provides a list of GPIB device messages categorized by function and also describes in detail these device messages arranged in alphabetical order, when the MU368030A Universal Modulation Unit installed with the MX368033A CDMA2000 1xEV-DO Signal Generation Software is mounted in the MG3681A Digital Modulation Signal Generator.

For further description of remote control, refer to Section 4 “Remote Control” in the MG3681A Main Unit Operation Manual.

5.1 List of Device Messages Categorized by Function

Command and query messages

The header portion of the command message is a reserved word represented by capital alphanumeric characters. The end of a query message header contains an interrogation mark (?). In the argument part of command and query messages, multiple arguments can be separated with a separator (,). Arguments are described below.

[1] Capitals : Reserved word

[2] Numerals : Reserved word

[3] Small letters in argument part:

f (Frequency) : Numeric data (NR1, NR2, NR3)

Suffix code : GHZ, GZ, MHz, MZ, kHz, KZ, HZ
When the unit is omitted, HZ is assumed.

l (level) (relative value) : Numeric data (NR1, NR2, NR3 format)

Suffix code : dB
When the unit is omitted, dB is assumed.

n (integer without unit) : Numeric data (NR1 format)

r (real number without unit) :
Numeric data (NR2 format)

h (hexadecimal number without unit) :
Numeric data (hexadecimal number)

s (character string) : Alphanumeric characters enclosed in double quotation marks (“ ”) or single quotation marks (‘ ’).

Device messages list

<Common>

Items	Device messages		
Control Items	**Command messages**	**Query messages**	**Response messages**
I/Q Source Internal	MODE INT IQSRC INT	MODE? IQSRC?	MODE INT IQSRC INT
I/Q Source External	MODE EXT IQSRC EXT	MODE? IQSRC?	MODE EXT IQSRC EXT
I/Q Source OFF	MODE OFF IQSRC OFF	MODE? IQSRC?	MODE OFF IQSRC OFF
System 1XEV-DO	SYS 1XEV-DO	SYS?	SYS 1XEV-DO
Baseband ON	BASEBAND ON	BASEBAND?	BASEBAND ON
Baseband OFF	BASEBAND OFF	BASEBAND?	BASEBAND OFF
PM ON	PMO ON	PMO?	PMO ON
PM OFF	PMO OFF	PMO?	PMO OFF

<Modulation>

Items	Device messages		
Control Items	**Command messages**	**Query messages**	**Response messages**
Wave Data Restart	DLRES	—	—
Wave Data Download	DOWNLOAD	—	—
Pattern	PAT n n: 0 to 23	PAT?	PAT n,s
Reference Clock Source	REFCLK INT	REFCLK?	REFCLK INT
Reference Clock Source	REFCLK EXT	REFCLK?	REFCLK EXT
Reference Clock Source	REFCLK EXT2	REFCLK?	REFCLK EXT2
Start Trigger Delay	STDLY n n: 0 to 16777215	STDLY?	STDLY n
Start Trigger Source	STGS INT	STGS?	STGS INT
Start Trigger Source	STGS EXT	STGS?	STGS EXT
Start Trigger Source	STGS EXTSTA	STGS?	STGS EXT
Start Trigger Source	STGS EXTFRM	STGS?	STGS EXTFRM

5.2 Details of Device Messages in Alphabetical Order

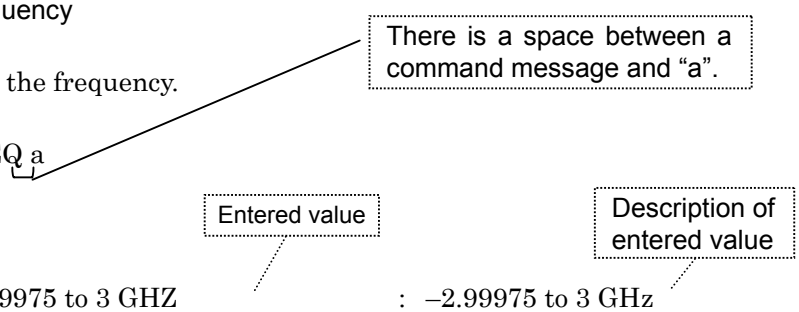
<Examples>

FREQ

Frequency

Function Sets the frequency.

Command message FREQ a



Value of a	–2.99975 to 3 GHZ	:	–2.99975 to 3 GHz
	–2999.75 to 3000 MHZ	:	–2999.75 to 3000 MHz
	–2999750 to 3000000 KHZ	:	–2999750 to 3000000 kHz
	–2999750000.00 to 3000000000 HZ	:	–2999750000.00 to 3000000000 Hz

Query message FREQ?

Response message FREQ a

Example FREQ 123MHZ

BASEBAND

Baseband (On/Off)

Function	Sets baseband On/Off.
Command message	BASEBAND a
Value of a	ON : Baseband On OFF : Baseband Off
Query message	BASEBAND?
Response message	BASEBAND a
Example	BASEBAND ON

DLRES

Wave Data Restart

Function Re-synchronizes with the external trigger in the start trigger mode.

Command message DLRES

Example DLRES

DOWNLOAD

Wave Data Download

Function Downloads the modulation wave and switches the output modulation wave.

Command message DOWNLOAD

IQSRC

I/Q Source

Function Selects the modulation source for digital modulation.

Command message IQSRC a

Value of a
INT : Internal (internal modulation unit)
EXT : External (external input)
OFF : I/Q modulation stop (only pulse modulation enabled)

Query message IQSRC?

Response message IQSRC a

Example IQSRC INT

PAT

Pattern

Function Selects the 1xEV-DO modulation signal.

Command message PAT n

Value of n 0 to 23

Query message PAT?

Response message PAT n,s

Restrictions “n” shows the1xEV-DO modulation signal number and “s“ shows the name of 1xEV-DO modulation signal. As for the1xEV-DO modulation signal corresponding to “n” and “s”, refer to “1xEV-DO Modulation Signal List” in Section 3.1.1.

Example PAT 2

PMO

Pulse-Modulation

Function Sets On/Off and Internal/External of pulse modulation.

Command message PMO a

Value of a
INT : Internal (generates with modulation unit)
EXT : External (uses external device signal)
OFF : Off (signals always exist)

Query message PMO?

Response message PMO a

Example PMO INT

REFCLK

Reference Clock Source

Function Selects the baseband reference timing (external or internal).

Command message REFCLK a

Value of a
INT : Internal selection
EXT : External (TTL) selection
EXT2 : External 2 (AC: 5 Vp-p) selection

Query message REFCLK?

Response message REFCLK a

Example REFCLK INT

STDLY

Start Trigger delay amount

Function	Sets the RF signal output timing.
Command message	STDLY n
Value of n	0 to 16777215
Query message	STDLY?
Response message	STDLY n
Example	STDLY 10

STGS

Start Trigger Source

Function	Sets Trigger Source.	
Command message	STGS a	
Value of a	INT	: Internal trigger mode
	EXTSTA, EXT	: Start trigger mode
	EXTFRM	: Frame trigger mode
Query message	STGS?	
Response message	STGS a	
Example	STGS INT	

SYS

System

Function Sets the digital modulation system.

Command message SYS a

Value of a
NONE : Digital modulation system not mounted.
1XEV-DO : CDMA2000 1xEV-DO Signal Generation Software

Query message SYS?

Response message SYS a

Example SYS 1XEV-DO

Section 6 Performance Test

This section describes the performance test when MX368033A CDMA2000 1xEV-DO Signal Generation Software is installed on the MU368030A Universal Modulation Unit, which is mounted on the MG3681A Digital Modulation Signal Generator. In order to implement the performance test as preventive maintenance, information such as required measuring instrument, setup procedure, and test procedures are included.

6.1 Performance Test

6.1.1 About the performance test

The performance test explained here is implemented as part of preventive maintenance against performance deterioration of the instrument. You are advised to implement a performance test whenever necessary, for examples, upon acceptance inspection, regular inspection, and post-repair performance confirmation. If you find an item, which does not meet specifications during a performance test, please contact Anritsu Corporation or one of our dealers.

The performance test consists of the following items:

- Output level accuracy

Be sure to implement periodically the performance test for items considered important as preventive maintenance. We recommend that the performance inspection is executed regularly once or twice a year.

In addition, it is recommended that the results are summarized using the Appendix C “Performance Test Record.”

CAUTION

Unless otherwise specified, be sure to warm up the device to be tested and the measuring instruments for at least 30 minutes or over until they become stable, before implementing the performance test. To ensure the maximum measurement accuracy, we recommend that you observe the above as well as keeping the room temperature, limiting AC power voltage fluctuations to a minimum, and making sure that there are no problems with noise, vibration, dust, humidity or other environmental factors.

6.1.2 Instruments required for the performance test

A list of instruments required for the performance test is shown below.

Test Item	Recommended Instrument	Anritsu Model Name
Output level accuracy	Power meter	ML4803A
	Power sensor	MA4601A

6.2 Output Level Accuracy

Test specifications

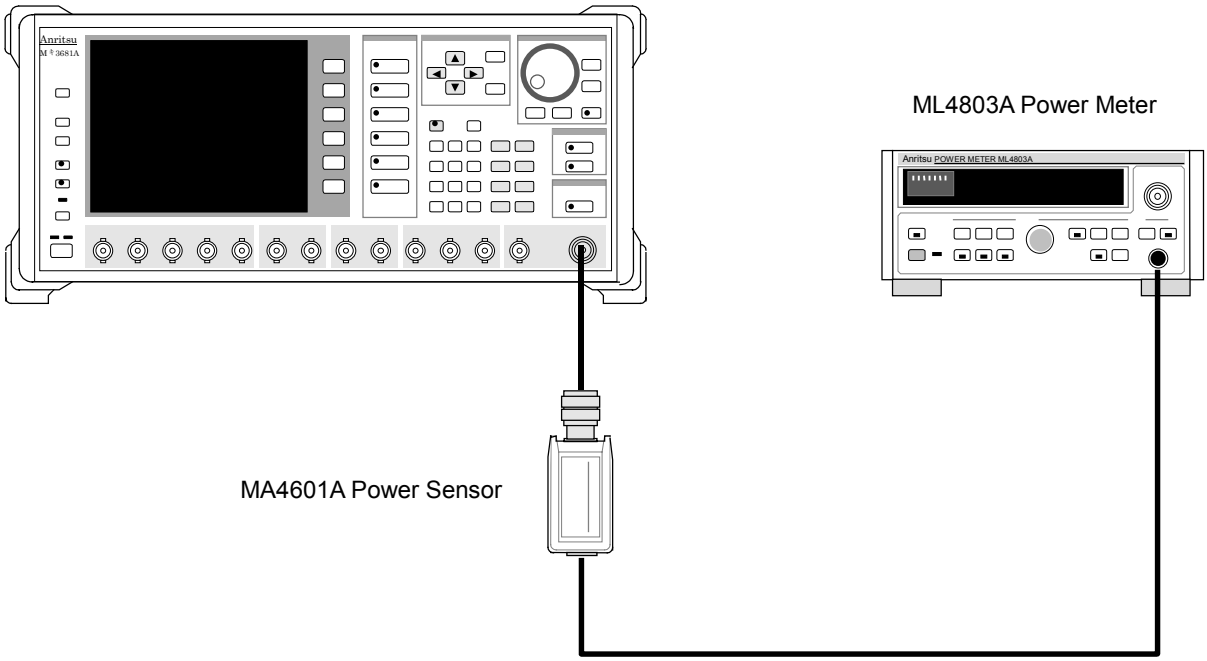
Difference from output level at CW	±1.5 dB

Conditions

RF output level	≤–3 dBm
Carrier frequency	10 to 3000 MHz
Level continuous mode	Off

Test procedure

MG3681A
+ MU368030A (Universal Modulation Unit)
+ MX368033A (CDMA2000 1xEV-DO Signal Generation Software)



[1] Set the modulation parameter of MG3681A as shown below:

Preset	: —
Baseband	: On
I/Q Mod	: Int
Digital Modulation	: On
System	: 1XEV-DO
Pattern	: Measured 1xEV-DO modulation signal

[2] Set RF Output of MG3681A to Off.

[3] Perform adjustment of zero point and calibrate sensor sensitivity of Power meter.

[4] Set the output level of MG3681A to measured value. (In the above system, the measurement-enabled minimum level depends on the sensitivity of power sensor.)

[5] Set the calibration coefficient of sensor in the power meter.

[6] Set the Digital Modulation of the MG3681A to Off, and measure the output level of the MG3681A at CW.

[7] Set the Digital Modulation to On, and measure the output level of the MG3681A in modulating.

[8] Confirm that difference between the output level at CW and the output level in modulating is within specification.

Appendix

Appendix A Specifications

When installed in MU368030A mounted on MG3681A

Item		Specifications
Corresponding system/Modulation system		CDMA2000 1xEV-DO : Corresponding specifications 3GPP2 C.S0024 Forward channel : 16QAM, 8PSK, QPSK (Data), QPSK (Spreading) Reverse channel : BPSK (Data), HPSK (Spreading)
Baseband Filter		Reverse channel : FIR filter according to IS-95 Forward channel : FIR filter with equalizer according to IS-95
Modulation data	Forward common	Channel configuration : Pilot channel, Traffic channel, Time division multiplex of MAC channel Pilot channel : All 0, Walsh cover=0 Traffic channel : Packet data PN15fix (4 Frame, without Idle slot) MAC channel RPC bit of RPC channel : Head slot of frame is All "1", the others are All "0". Channel power=–11.46 dB RA bit of RA channel : All 0, Channel power=–11.46 dB Or, the following MAC channel RPC bit of RPC channel : Random, channel power=–12.04 dB RA bit of RA channel : Random, channel power=–11.42 dB
	Forward 38.4 kbps, 16 slots	Preamble : 1024-bit MAC Index : 4 (RA channel), 5 to 17 (RPC channel) Traffic channel : QPSK modulation, Data rate=38.4 kbps, Number of time division multiplex 16 slots
	Forward 76.8 kbps, 8 slots	Preamble : 512-bit MAC Index : 4 (RA channel), 5 to 17 (RPC channel) Traffic channel : QPSK modulation, Data rate=76.8 kbps, Number of time division multiplex 8 slots
	Forward 153.6 kbps, 4 slots	Preamble : 256-bit MAC Index : 4 (RA channel), 5 to 17 (RPC channel) Traffic channel : QPSK modulation, Data rate=153.6 kbps, Number of time division multiplex 4 slots
	Forward 307.2 kbps, 2 slots	Preamble : 128-bit MAC Index : 4 (RA channel), 5 to 17 (RPC channel) Traffic channel : QPSK modulation, Data rate=307.2 kbps, Number of time division multiplex 2 slots
	Forward 614.4 kbps, 1 slot	Preamble : 64-bit MAC Index : 4 (RA channel), 5 to 17 (RPC channel) Traffic channel : QPSK modulation, Data rate=614.4 kbps, Number of time division multiplex 1 slot

Note:

Channel power is the value where the pilot channel power is set to 0 dB.

Item		Specifications	
Modulation data	Forward 307.2 kbps, 4 slots	Preamble MAC Index Traffic channel	: 128-bit : 4 (RA channel), 5 to 17 (RPC channel) : QPSK modulation, Data rate=307.2 kbps, Number of time division multiplex 4 slots
	Forward 614.4 kbps, 2 slots	Preamble MAC Index Traffic channel	: 64-bit : 4 (RA channel), 5 to 17 (RPC channel) : QPSK modulation, Data rate=614.4 kbps, Number of time division multiplex 2 slots
	Forward 1228.8 kbps, 1 slot	Preamble MAC Index Traffic channel	: 64-bit : 4 (RA channel), 5 to 17 (RPC channel) : QPSK modulation, Data rate=1228.8 kbps, Number of time division multiplex 1 slot
	Forward 921.6 kbps, 2 slots	Preamble MAC Index Traffic channel	: 64-bit : 4 (RA channel), 5 to 17 (RPC channel) : 8PSK modulation, Data rate=921.6 kbps, Number of time division multiplex 2 slots
	Forward 1843.2 kbps, 1 slot	Preamble MAC Index Traffic channel	: 64-bit : 4 (RA channel), 5 to 17 (RPC channel) : 8PSK modulation, Data rate=1843.2 kbps, Number of time division multiplex 1 slots
	Forward 1228.8 kbps, 2 slots	Preamble MAC Index Traffic channel	: 64-bit : 4 (RA channel), 5 to 17 (RPC channel) : 16QAM modulation, Data rate=1228.8 kbps, Number of time division multiplex 2 slots
	Forward 2457.6 kbps, 1 slot	Preamble MAC Index Traffic channel	: 64-bit : 4 (RA channel), 5 to 17 (RPC channel) : 16QAM modulation, Data rate=2457.6 kbps, Number of time division multiplex 1 slot
	Forward Idle slot	MAC Index	: 4 (RA channel), 5 to 17 (RPC channel)

Item		Specifications	
Modulation data	Reverse common	DRC channel	: "0001", DRC cover symbol "0", Channel power=3.0 dB
		RRI channel	: Channel power=0.0 dB
		Long code mask	: MI=3FF00000000 (16 Hex.), MQ=3FE00000001 (16 Hex.)
		Data channel	: PN9fix data (1 frame length)
	Reverse 9.6 kbps	Data channel	: Data rate=9.6 kbps, Channel power=3.75 dB
		RRI symblol	: "001"
		ACK channel	: All 0, Channel power=3.0 dB
	Reverse 19.2 kbps	Data channel	: Data rate=19.2 kbps, Channel power=6.75 dB
		RRI symbol	: "010"
		ACK channel	: All 0, Channel power=3.0 dB
	Reverse 38.4 kbps	Data channel	: Data rate=38.4 kbps, Channel power=9.75 dB
		RRI symbol	: "011"
		ACK channel	: All 0, Channel power=3.0 dB
	Reverse 76.8 kbps	Data channel	: Data rate=76.8 kbps, Channel power=13.25 dB
		RRI symbol	: "100"
		ACK channel	: All 0, Channel power=3.0 dB
	Reverse 153.6 kbps	Data channel	: Data rate=153.6 kbps, Channel power=18.50 dB
		RRI symbol	: "101"
		ACK channel	: All 0, Channel power=3.0 dB
	Reverse 9.6 kbps_RT	Data channel	: Data rate=9.6 kbps, Channel power=3.75 dB
		RRI symbol	: "001"
		ACK channel	: All 0, Channel power=0.0 dB
	Reverse 19.2 kbps_RT	Data channel	: Data rate=19.2 kbps, Channel power=6.75 dB
		RRI symbol	: "010"
		ACK channel	: All 0, Channel power=0.0 dB
	Reverse 38.4 kbps_RT	Data channel	: Data rate=38.4 kbps, Channel power=9.75 dB
		RRI symbol	: "011"
		ACK channel	: All 0, Channel power=0.0 dB
	Reverse 76.8 kbps_RT	Data channel	: Data rate=76.8 kbps, Channel power=13.25 dB
		RRI symbol	: "100"
		ACK channel	: All 0, Channel power=0.0 dB
	Reverse 153.6 kbps_RT	Data channel	: Data rate=153.6 kbps, Channel power=18.50 dB
		RRI symbol	: "101"
		ACK channel	: All 0, Channel power=0.0 dB

Note:

Channel power is the value where the pilot channel power is set to 0 dB.

Item		Specifications
RF signal	Frequency range	10 to 3000 MHz
	Level range	–143 to 5 dBm
	Level accuracy	±1.5 dB or less (≤–3 dBm) for output level as against CW
	Spurious emission	In the range from 100 to 2300 MHz, ratio of all power at –3 dBm output to power in 30 kHz bandwidth (PLL mode: Normal) ≤–65 dBc (885 kHz to 1.98 MHz offset), ≤–70 dBc (1.98 to 2.5 MHz offset), ≤–77 dBc (2.5 to 5.0 MHz offset) (Note: Performance degradation caused by Spurious from MG3681A is excluded.)
IQ signal	Output level	Forward 38.4 kbps 16 slots : 149 mV (rms) Forward 76.8 kbps 8 slots : 149 mV (rms) Forward 153.6 kbps 4 slots : 149 mV (rms) Forward 307.2 kbps 2 slots : 149 mV (rms) Forward 614.4 kbps 1 slot : 149 mV (rms) Forward 307.2 kbps 4 slots : 149 mV (rms) Forward 614.4 kbps 2 slots : 149 mV (rms) Forward 1228.8 kbps 1 slot : 149 mV (rms) Forward 921.6 kbps 2 slots : 149 mV (rms) Forward 1843.2 kbps 1 slot : 149 mV (rms) Forward 1228.8 kbps 2 slots : 149 mV (rms) Forward 2457.6 kbps 1 slot : 149 mV (rms) Forward idle slot : 149 mV (rms) Reverse 9.6 kbps : 252 mV (rms) Reverse 19.2 kbps : 254 mV (rms) Reverse 38.4 kbps : 269 mV (rms) Reverse 76.8 kbps : 199 mV (rms) Reverse 153.6 kbps : 301 mV (rms) Reverse 9.6 kbps_RT : 252 mV (rms) Reverse 19.2 kbps_RT : 254 mV (rms) Reverse 38.4 kbps_RT : 269 mV (rms) Reverse 76.8 kbps_RT : 199 mV (rms) Reverse 153.6 kbps_RT : 301 mV (rms)

Item		Specifications
Trans-mission speed	Chip rate	1.2288 Mcps
	Transmission speed accuracy	Depends on reference signal accuracy of MG3681A (Excluded in external synchronizing)
Start trigger		Inputs Start Trigger from outside. Provided with delay adjusting function of output for external trigger. (Delay adjusting function: ranging from 0 to 16777215, resolution of chips/8) Front BNC connector, TTL level
Firmware in use Back-up area		CPU: 137.3 kBytes, FPGA: 49.5 kBytes

PN9fix, PN15fix: Data with constant length (such as 3-frame length) where repeat of PN sequence is not continuous,

Appendix B List of Initial Value

Setting	Initial Value
Digital Modulation Main Screen	
Pattern	0: FWD_38.4_16_MR
Trigger Source	Int
Trigger Delay	0/8 cps (0.0000 cps)
Reference Clock	Int

Appendix C Performance Test Record

Tested at:_____ Report No. _____

_____ Date _____

_____ Tested by _____

Product Name MG3681A Digital Modulation SG
+MU368030A Universal Modulation Unit
+MX368033A CDMA2000 1xEV-DO Signal Generation Software

Serial No. _____ Ambient temperature _____°C

AC Power frequency _____Hz Relative Humidity _____%

Remarks:

_____

_____

_____

_____

Output level Accuracy (Section 6.2)

1xEV-DO Modulation Wave	Setting Output Level	Result					Specifications Maximum
		MHz	MHz	MHz	MHz	MHz	
FWD 38.4 kbps 16 slots	dBm						±1.5 dB
FWD 76.8 kbps 8 slots	dBm						±1.5 dB
FWD 153.6 kbps 4 slots	dBm						±1.5 dB
FWD 307.2 kbps 2 slots	dBm						±1.5 dB
FWD 614.4 kbps 1 slot	dBm						±1.5 dB
FWD 307.2 kbps 4 slots	dBm						±1.5 dB
FWD 614.4 kbps 2 slots	dBm						±1.5 dB
FWD 1228.8 kbps 1 slot	dBm						±1.5 dB
FWD 921.6 kbps 2 slots	dBm						±1.5 dB
FWD 1843.2 kbps 1 slot	dBm						±1.5 dB
FWD 1228.8 kbps 2 slots	dBm						±1.5 dB
FWD 2457.6 kbps 1 slot	dBm						±1.5 dB
RVS 9.6 kbps	dBm						±1.5 dB
RVS 19.2 kbps	dBm						±1.5 dB
RVS 38.4 kbps	dBm						±1.5 dB
RVS 76.8 kbps	dBm						±1.5 dB
RVS 153.6 kbps	dBm						±1.5 dB

1xEV-DO Modulation Wave	Setting Output Level	Result					Specifica-tions Maximum
		MHz	MHz	MHz	MHz	MHz	
RVS 9.6 kbps_RT	dBm						±1.5 dB
RVS 19.2 kbps_RT	dBm						±1.5 dB
RVS 38.4 kbps_RT	dBm						±1.5 dB
RVS 76.8 kbps_RT	dBm						±1.5 dB
RVS 153.6 kbps_RT	dBm						±1.5 dB

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